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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,891	11/04/2003	Howard S. Landis	BUR920030033US2	2890

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,891	LANDIS, HOWARD S.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/19/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-17 and 30-31 in the reply filed on 11/19/2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

Claims 11 and 12 are objected to because of the following informalities: "a level" should be -- the level--. Appropriate correction is required.

Claim Rejections - 35-8 USC § 102

The following is a quotation of the appropriate paragraphs of 35-8 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 14, 17 and 30 are rejected under 35-8 U.S.C. 102(b) as being anticipated by Numata et al..

Regarding claim 1, Numata et al. discloses on figures 5-8 a semiconductor structure formed on a substrate 112 comprising a first rigid dielectric layer 118; a first non-rigid dielectric layer wiring level 116 formed on the first rigid dielectric layer having

at least one interconnect 114; a second rigid dielectric layer 118 (upper layer 118) formed on the first non-rigid dielectric wiring level; and a structural securing means 114 (note that a so-called structural securing means is merely a label such that element 114 of Numata et al. can be labeled as a structural securing means) associated with the non-rigid dielectric wiring level 116 for preventing a portion of the first or second rigid dielectric layers adjacent the interconnect from de-layering from the interconnect.

Regarding claim 2, Numata et al. discloses on figures 5-8 the structural securing means 114 comprises at least one dummy fill shape in proximity to the interconnect having a coefficient of thermal expansion (CTE) better matched to the first and second rigid dielectric layer than that of the non-rigid dielectric wiring level.

Note that element 114 is formed of alloy of copper (table 1), the first and second rigid dielectric 118 formed of silicon dioxide (table 1) and the non rigid dielectric layer 116 formed of fluorinated silicon oxide (table 1). As such, the coefficient of thermal expansion of alloy of copper is better matched to silicon dioxide than to fluorinated silicon oxide.

Regarding claim 3, Numata et al. discloses on figures 5-8 the at least one dummy fill shape 114 is one of an alloy predominately composed of copper (table 1).

Regarding claim 4, Numata et al. discloses on figures 5-8 an effective CTE of a region of the first non-rigid dielectric wiring level 116 is reduced in proportion to a density of the at least one dummy metal fill shape. Note that the dummy fill shape is formed within the non-rigid dielectric wiring level, and therefore, the effective CTE of a

region of the first non-rigid dielectric wiring level should be reduced with the presence of the dummy metal fill shape (a different material).

Regarding claim 5, Numata et al. discloses on figures 5-8 the structural securing means 114 are a plurality of dummy fill shapes aligned in rows and columns about the interconnect.

Regarding claim 6, Numata et al. discloses on figures 5-8 the structural securing means 114 is matched to an overall average local metal density such that CTE mismatch stresses and deflections are substantially toward zero. The device of Numata et al. would function in the same manner since it encompassed the same structure and material as the claimed invention.

Regarding claim 7, Numata et al. discloses on figures 5-8 the structural securing means 114 reduces temperature driven stress. The structural securing means is metal that conducts heat and relieves heat driven stress accordingly.

Regarding claim 8; Numata et al. discloses on figures 5-8 the structural securing means 114 inhibits deflecting of the first and second rigid dielectric layer 118.

Regarding claim 14, Numata et al. discloses on figure 8 the structural means 114 are dummy fill shapes arranged in a staggered offset pattern surrounding interconnect.

Regarding claim 17, Numata et al. discloses on figure 8 the structural securing means 114 are plurality of square shaped fill dummy shapes arranged in a staggered pattern in the first non-rigid dielectric wiring level 116.

Regarding claim 30, Numata et al. discloses on figures 5-8 a process of forming a semiconductor structure comprising forming a first rigid dielectric layer 118; forming a

first non-rigid dielectric layer wiring level 116 on the first rigid dielectric layer having at least one interconnect 114; forming a second rigid dielectric layer 118 (upper layer 118) formed on the first non-rigid dielectric wiring level; and forming a plurality of dummy metal fill shapes 114 (note that a so-called structural securing means is merely a label such that element 114 can be labeled as a structural securing means) in the non-rigid dielectric wiring level in proximity to the interconnect for preventing a portion of the first or second rigid dielectric layers adjacent the interconnect from de-layering from the interconnect.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-14, 17, 31 rejected under 35 U.S.C. 103(a) as being unpatentable over Numata et al. as applied to claims 1 and 30 above.

Regarding claim 9, Numata et al discloses on figures 5-8 substantially all the structure set forth in the claimed invention except the interconnect having a line width from 0.1 microns to grater than 1 micron. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having the interconnect having a line width from 0.1 microns to grater than 1 micron for the purpose of providing a specific layout of a semiconductor structure, since it has

been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 10, Numata et al discloses on figures 5-8 substantially all the structure set forth in the claimed invention except a minimum spacing between the dummy fill shapes being one to four times a maximum spacing for the level. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having a minimum spacing between the dummy fill shapes being one to four times a maximum spacing for the level for the purpose of providing a specific layout of a semiconductor structure, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 11, Numata et al discloses on figures 5-8 substantially all the structure set forth in the claimed invention except a minimum spacing between the dummy fill shapes being equal to a minimum spacing width for the level. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having a minimum spacing between the dummy fill shapes being equal to a minimum spacing width for the level for the purpose of providing a specific layout of a semiconductor structure, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the

optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 12 and 31, Numata et al discloses on figures 5-8 substantially all the structure set forth in the claimed invention except a density of the dummy fill shapes being between approximately 45% and 50%. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having a density of the dummy fill shapes being between approximately 45% and 50% for the purpose of providing a specific layout of a semiconductor structure, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 13, Numata et al discloses on figures 5-8 substantially all the structure set forth in the claimed invention except a width and length of the dummy fill shape being 3X a minimum line width of the interconnect. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having a width and length of the dummy fill shape being 3X a minimum line width of the interconnect for the purpose of providing a specific layout of a semiconductor structure, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Numata et al. as applied to claim 1 above, and further in view of Wang et al.

Regarding claim 15, Numata et al. discloses on figures 5-8 substantially all the structures set forth in the claimed invention except the first non-rigid dielectric wiring level being a low k dielectric siloxane based semi-organic layer. Note that Numata et al teaches that the first non-rigid dielectric wiring level 116 is organic spin on glass. Wang et al teaches that the dielectric layer can be alternatively formed of spin on glass or siloxane based semi-organic ([0100]). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numata et al. by having the first non-rigid dielectric wiring level being a low k dielectric siloxane based semi-organic layer for the purpose of providing a specific application to a semiconductor structure.

Regarding claim 16, Numata et al. discloses on figures 5-8 the first and second rigid dielectric layer 118 contain silicon oxide based glass (table 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for

the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
December 10, 2004.

ALLAN R. WILSON
PRIMARY EXAMINER